Abstract

DNL and INL errors are minimized in a pipelined converter that is arranged to use reference pre-sampling. An example first stage in the pipelined converter includes a sample/hold amplifier (SHA) circuit, an evaluator circuit, and a multiplying digital-to-analog converter (MDAC) circuit. The evaluator circuit evaluates the input signal in the converter while the SHA circuit samples the input signal. The MDAC samples the SHA output at substantially the same time it samples a reference voltage, where the reference voltage is adjusted in response to the output of the evaluator circuit. Errors due to capacitor mismatching are minimized such that the settling characteristics of the various amplifiers in the circuits dominate the DNL/INL performance.

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